IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Jarrett L. RINALDI, et al.

Serial No.:	09/965,234	Group Art Unit:	2827
Filed:	September 25, 2001	Examiner:	J. Mitchell
FOR:	MULTI-STACK SURFACE MOUNT LIGHT EMITTING DIODES		

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits this brief on appeal, thus perfecting the notice of appeal filed on December 4, 2003. A petition for a one month extension of time is submitted herewith.

The headings and subject matter under rule 192 follow.

(1) Real Party in Interest

This case is assigned of record to Intel Corporation, who is the real party in interest.

(2) Related Appeals and Interferences

There are no known related appeals and / or interferences.

(3) Status of Claims

Claims 21-31 are pending in the case and stand rejected.

(4) Status of Amendments

No amendments have been made after the final rejection.

(5) Summary of Invention

Some embodiments of the claims generally relate to a surface mount LED package that include two or more die from the same integrated circuit wafer. In some claims, the die are integrally connected adjacent die from the same wafer. In a multi-stack LED package, using the integrally connected adjacent die of the present invention reduces the number of times the wafer needs to be cut and also simplifies the assembly process, as compared to the prior art multi-stack LED package which utilizes separately cut die for each LED.

(6) Issues

I. The rejection of claim 21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, is in error.

II. The rejection of claims 21-23, 25-27, and 29-31 under 35 U.S.C. § 102(e) as being anticipated by Ishinaga (U.S. Patent No. 6,093,940) is in error.

III. The rejection of claims 24 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Ishinaga is in error.

(7) Grouping of the Claims

Group I: Claims 21-23 stand or fall together;

Group II: Claims 25-27 stand or fall together;

Group III: Claim 29 stands or falls on its own;

Group IV: Claim 30 stands or falls on its own;

Group V: Claim 31 stands or falls on its own;

Group VI: Claim 24 stands or falls on its own;

Group VII: Claim 28 stands or falls on its own;

(8) Argument

I. The rejection of claim 21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, is in error.

The office action asserts that the specification does not describe "a plurality of light emitting diode die formed on the integrated circuit substrate" in such a way as to reasonably convey to one skilled in the art that the applicants were in possession of the claimed invention at the time the application was filed. This is simply incorrect.

Reference is made throughout the specification to an LED wafer together with various combinations of two or more LEDs on the wafer (e.g. see Fig. 4 and related description). Accordingly, there is ample support in the specification for a plurality of light emitting diode die (e.g. two or more LEDs) formed on the integrated circuit substrate (e.g. the LED wafer). Literal support for the choice of wording is not required and support may be provided by the figures and what one of ordinary skill in the art would appreciate. For example, on page 6, line 10-11 refer to manufacturing the packages with "a standard LED wafer." At the time the application filed, one skilled in the art would understand a "wafer" to be an integrated circuit substrate. At the time the application was filed, one of ordinary skill in the art would appreciate the wafer 38 in Fig. 4 to be an integrated circuit substrate having a plurality of LED die formed thereon.

Accordingly, applicants submit that claim 21 is in proper form under 35 U.S.C. § 112, first paragraph because the specification satisfactorily conveys to one of ordinary skill in the art that the applicants were in possession of the invention as claimed, including a plurality of light emitting diode die formed on the integrated circuit substrate. The rejection should be reversed

II. The rejection of claims 21-23, 25-27, and 29-31 under 35 U.S.C. § 102(e) as being anticipated by Ishinaga (U.S. Patent No. 6,093,940) is in error.

The Examiner fails to comply with 37 C.F.R. § 104 (c)(2), because the office action does not sufficiently designate the particular part of the reference relied upon for disclosing each claim recitation and the interrelationships between the claim elements.

The Office Action lacks sufficient clarity to understand which portions of the references are relied upon for each claim element. In a single paragraph, paragraph 5 of the final office action, the Examiner rejects nine different claims without actually identifying any single claim with particularity. The Examiner completely ignores most of the connecting language between claim recitations. In doing so, the Examiner conflates the references and the claims without clearly identifying how the reference allegedly teaches various aspects of the claims. Applicants are not required to guess as to how the reference is being applied to the claim.

In the Advisory Action mailed, January 28, 2004, the Examiner's single sentence response to Applicants' arguments fails to improve the clarity of the rejection.

To the extent that the Office Action fails to satisfactorily identify the portions of the cited references which are being asserted against the claim elements, the Office Action fails to establish anticipation of the claim.

In order to anticipate, the reference must identically disclose each and every claim element. The Examiner has not met the burden of establishing how each and every claim element is disclosed by the reference. Accordingly, the rejection should be reversed.

With respect to Group I, claims 21-23:

The Examiner fails to establish anticipation of claim 21. Claim 21 recites a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit substrate. Ishinaga fails to teach or suggest this recited claim feature.

In contrast to the invention as recited in claim 21, Ishinaga teaches only the conventional arrangement, wherein a plurality of separate LED die are utilized in an LED package. Substrate 1 disclosed in Ishinaga is not an integrated circuit substrate, as that term would be understood in the art. Rather, the substrate 1 of Ishinaga would be considered a packaging substrate.

Moreover, the two LEDs in Ishinaga are not formed on the substrate 1, rather they are affixed to the substrate 1. Ishinaga discloses that "the two LED elements 2a and 2b are individually fixed" on the substrate (see col. 1, lines 35-37).

As noted in the specification, there are numerous cost and manufacturing advantages to the device structure recited in claim 21. None of these cost or manufacturing advantages are taught or suggested by Ishinaga.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit substrate, claim 21 and its dependent claims are not anticipated by and are patentable over Ishinaga, and the rejection should be reversed.

Claims 22-23 depend either directly or indirectly from claim 21 and, in the interest of judicial economy, are not argued separately.

With respect to Group II, claims 25-27:

The Examiner fails to establish anticipation of claim 25. Claim 25 recites a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single wafer. For the reasons given above, the die disclosed in Ishinaga are not integrally connected, are not adjacent, and do not come from a single wafer. Accordingly, the § 102 rejection must be reversed. As noted above, there are numerous cost and manufacturing advantages to the device structure recited in claim 25. None of these cost or manufacturing advantages are taught or suggested by Ishinaga, and claim 25 is therefore patentable over Ishinaga.

Applicants do not understand the Examiner's statement on page 3, lines 10-11 that "a die inherently form a single wafer;" Assuming the Examiner means die "from" a single wafer, this is not inherent because the conventional arrangement may utilize die from different wafers. Assuming the Examiner means that a single die itself forms a single wafer, this has no bearing the claim language that recites a plurality of integrally connected adjacent die from a single wafer.

With respect to paragraph 6 of the office action, the Examiner's argument is not understood because there are no product-by-process claims pending in the present application. The recitation "adjacent die from a single wafer" describes a structural relationship, not a process.

In fact, Ishinaga teaches away from using a plurality of die from the same substrate. Ishinaga is directed to a two color LED package which uses two different color

LED elements (2a is red and 2b is green, see col. 1, lines 65-67). Accordingly, the two die 2a and 2b do not come from the same substrate.

With respect to paragraph 13 of the final office action, the Examiner asserts that applicant has not established a prima facie that dies from a single wafer cannot have different colors. However, applicant has no such burden. It is well established law that applicants are entitled to their patent unless the Patent Office establishes evidence to the contrary. Applicants note that the publication US 20020030444 cited for support for the Examiner's position that "LEDs of same wafer that emit different color" is not properly of record in this case. In any event, the Examiner misconstrues the publication, which merely describes that an underlying wafer may be processed to deposit thin films on the wafer which change the color emitted by the LEDs on the wafer. However, all die from the processed wafer emit the same color (in fact uniformity in color appears to be the object of the publication).

Applicants disagree with the Examiner's assertion that "adjacent die from a single wafer" does not describe a structural relationship except that the LED has a substrate. First the Examiner ignores the language "integrally connected" which further describes the structural relationship. Taken as whole, one of ordinary skill in the art would understand the phrase to indicate two or more adjacent die from the same wafer which have not been cut or separated. It is improper for the Examiner to ignore the recited language or not give the language patentable weight.

Finally, with respect to paragraph 14 of the office action, the principle cited by the Examiner does not appear to have any bearing on the present application because the advantages provided by the present invention are simply not provided by any device described in Ishinaga. Moreover, the Examiner has not identified any suggestion of the prior art to "follow" from which the advantages would naturally flow. Applicants have not merely recognized another advantage provide by the device of Ishinaga. Rather, applicants have invented a new device which provides numerous cost and manufacturing advantages as compared to the device described by Ishinaga.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single wafer, claim 25 and its dependent claims are not anticipated by and are patentable over Ishinaga, and the rejection should be reversed.

Claims 26-27 depend either directly or indirectly from claim 25 and, in the interest of judicial economy, are not argued separately.

With respect to Group III, Claim 29:

Claim 29 depends directly from claim 21 and is accordingly patentable for at least the reasons given above with respect to claim 21. Claim 29 is separately patentable for at least the following reasons.

Claim 29 recites a reinforcing pin integrally formed on the outside of the integrated circuit substrate. Although the final office action is not clear, it appears that the Examiner is relying on the resin molding 6 disclosed in Ishinaga for allegedly identically disclosing the recited reinforcing pin. The Examiner is simply incorrect in his assertions of what Ishinaga discloses.

The final office action mentions "an inherent piece of long slender solid material, via a portion of 6 ..." on page 3, lines 12-13. Element 6 of the cited reference is described in Ishinaga as resin molding 6 (see col. 4, line 21). Applicants submit that resin molding is different from, does not identically disclose, and does not teach or suggest the recited reinforcing pin.

Because Ishinaga fails to teach or suggest a reinforcing pin, claim 29 is separately patentable and the rejection should be reversed.

With respect to Group IV, Claim 30:

Claim 30 depends directly from claim 29 and indirectly from claim 21 and is accordingly patentable for at least the reasons given above with respect to claims 21 and 29. Claim 30 is separately patentable for at least the following reasons.

The Examiner fails to establish anticipation of claim 30. Claim 30 recites a non-electrode reinforcing pin positioned between the cathode contact and the anode contact. The only cited portion of Ishinaga which even mentions a cathode or an anode (Fig. 3B, col. 5, lines 11-15) is completely devoid of any description related to the recited reinforcing pin (or even the resin molding 6). As noted above, the resin molding 6 (apparently relied upon by the Examiner for the reinforcing pin) is not a reinforcing pin. Moreover, the resin molding 6 does not appear to be positioned between any anode and /

or cathode contact on the device described in Ishinaga. Accordingly, the rejection is in error and should be reversed.

With respect to Group V, Claim 31:

Claim 31 depends directly from claim 25 and is accordingly patentable for at least the reasons given above with respect to claim 25. Claim 31 is separately patentable for at least the reasons given above with respect to claim 29.

III. The rejection of claims 24 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Ishinaga is in error.

With respect to Group VI, claim 24:

Claim 24 depends directly from claim 21, and is accordingly patentable for at least the reasons given above with respect to claim 21. Claim 24 is separately patentable for the following reasons.

The Examiner admits that the prior art fails to teach or suggest the recited array of die having at least two rows and two columns. The Examiner asserts, without support, that the recitation amounts to a mere duplication of essential working parts.

However, claim 24 is not directed to a mere duplication of elements, but more particularly to a novel arrangement of elements. Read together with its independent claim, the array of die are formed on the integrated circuit. In those applications where an array of LEDs are beneficial, the invention as recited in claim 24 provides even further advantages in terms of a reduced number of wafer cuts and simplified assembly. The result is not a mere duplication of parts, but rather a highly cost advantaged and more tightly integrated LED package.

Because the prior art admittedly fails to teach or suggest the recited array of die having at least two rows and two columns, and because the claim read as a whole is not a mere duplication of parts, claim 24 is separately patentable over Ishinaga.

With respect to Group VI, claim 28:

Claim 28 depends directly from claim 25, and is accordingly patentable for at least the reasons given above with respect to claim 25. Claim 28 is separately patentable for the following reasons.

The Examiner admits that the prior art fails to teach or suggest the recited array of die having at least two rows and two columns. The Examiner asserts, without support, that the recitation amounts to a mere duplication of essential working parts.

However, the claims are not directed to a mere duplication of elements, but more particularly to a novel arrangement of elements. Read together with its independent claim, the array of die are integrally connected adjacent die from a single wafer. In those applications where an array of LEDs are beneficial, the invention as recited in claim 28 provides even further advantages in terms of a reduced number of wafer cuts and simplified assembly. The result is not a mere duplication of parts, but rather a highly cost advantaged and more tightly integrated LED package.

Because the prior art admittedly fails to teach or suggest the recited array of die having at least two rows and two columns, and because the claim read as a whole is not a mere duplication of parts, claim 28 is separately patentable over Ishinaga.

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

March 3, 2004
Date

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APPENDIX OF CLAIMS

1-20. cancelled.

21. A surface mount light emitting diode package, comprising:

an integrated circuit substrate;

a plurality of light emitting diode die formed on the integrated circuit substrate; and

a plurality of electrical contacts on the outside of the integrated circuit substrate, said contacts adapted for surface mounting to a circuit board and providing electrical signals to said plurality of light emitting diode die.

22. The surface mount light emitting diode package as recited in claim 21, wherein the plurality of light emitting diode die comprise a stack of at least two die arranged in a line.

23. The surface mount light emitting diode package as recited in claim 22, wherein the line of die is adapted to form a right angle with respect to the circuit board when the package is mounted to the circuit board.

24. The surface mount light emitting diode package as recited in claim 21, wherein the plurality of light emitting diode die comprise an array of die having at least two rows and two columns.

25. A surface mount light emitting diode package, comprising:

a housing;

a plurality of light emitting diode die supported by the housing; and

a plurality of electrical contacts on the outside of the housing, said contacts adapted for surface mounting to a circuit board and providing electrical signals to said plurality of light emitting diode die,

wherein the plurality of die comprise integrally connected adjacent die from a single wafer.

26. The surface mount light emitting diode package as recited in claim 25, wherein the plurality of light emitting diode die comprise a stack of at least two die arranged in a line.

27. The surface mount light emitting diode package as recited in claim 26, wherein the line of die is adapted to form a right angle with respect to the circuit board when the package is mounted to the circuit board.

28. The surface mount light emitting diode package as recited in claim 25, wherein the plurality of light emitting diode die comprise an array of die having at least two rows and two columns.

29. The surface mount light emitting diode package as recited in claim 21, further comprising a reinforcing pin integrally formed on the outside of the integrated circuit substrate.

30. The surface mount light emitting diode package as recited in claim 29, wherein one of said plurality of electrical contacts comprises a cathode contact and wherein another of said plurality of electrical contacts comprises an anode contact, and wherein the reinforcing pin comprises a non-electrode reinforcing pin positioned between the cathode contact and the anode contact.

31. The surface mount light emitting diode package as recited in claim 25, further comprising a reinforcing pin formed on the integrally connected adjacent die.